LISTING OF THE CLAIMS

Pursuant to 37 C.F.R. §1.121, provided below is a listing of the claims of the present patent application.

1. (Currently Amended) An increment/decrement circuit for use with a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the increment/decrement circuit comprising:

a delay circuit block operable to receive and align ~~at least~~ a multi-bit block of said debug data;

a first mask circuit connected to said delay circuit block, wherein said first mask circuit is operable to select a first portion of said aligned, multi-bit block of ~~aligned~~ debug data; ~~for incrementing;~~

a second mask circuit connected to said delay circuit block, wherein said second mask circuit is operable to select a second portion of said aligned, multi-bit block of ~~aligned~~ debug data; ~~for decrementing;~~ and

an accumulation circuit connected to said first mask circuit and said second mask circuit, said accumulation circuit for

generating an accumulated value using said first portion and said second portion. ~~based on outputs provided by said first and second mask circuits.~~

2. (Currently Amended) The increment/decrement circuit as recited in claim 1, wherein said multi-bit block of said debug data comprises 16 bits.

3. (Currently Amended) The increment/decrement circuit as recited in claim 1, wherein said multi-bit block of said debug data forms a portion of an 80-bit wide debug data signal.

4. (Currently Amended) The increment/decrement circuit as recited in claim 1, wherein said delay circuit block is operable responsive to a delay_values signal that provides clock delaying values for each bit in said multi-bit block of said debug data.

5. (Original) The increment/decrement circuit as recited in claim 1, wherein said delay circuit block includes a series of registers operable to be tapped for providing a plurality of inputs to a Multiplexer (MUX) block that is controlled by a delay_values signal.

6. (Currently Amended) The increment/decrement circuit as recited in claim 1, wherein said first mask circuit comprises an AND block having a plurality of 2-input AND gates for bit-wise ANDing said aligned, multi-bit block of said debug data with a multi-bit inc_mask signal.

7. (Currently Amended) The increment/decrement circuit as recited in claim 1, wherein said first mask circuit comprises:

an XOR block having a plurality of XOR gates for bit-wise XORing said aligned, multi-bit block of said debug data with a multi-bit inc_invert signal to generate a multi-bit output signal; and

an AND block having a plurality of 2-input AND gates for bit-wise ANDing said multi-bit output signal with a multi-bit inc_mask signal.

8. (Original) The increment/decrement circuit as recited in claim 1, wherein said accumulation circuit comprises:

a first population count circuit coupled to said first mask circuit;

a second population count circuit coupled to said second mask circuit; and

an adder circuit coupled to said first population count circuit and said second population count circuit.

9. (Original) The increment/decrement circuit as recited in claim 1, wherein said accumulation circuit comprises:

a first population count circuit coupled to said first mask circuit;

a second population count circuit coupled to said second mask circuit; and

a subtract circuit coupled to said first population count circuit and said second population count circuit.

10. (Original) The increment/decrement circuit as recited in claim 1, wherein said accumulation circuit is operable to forward a signal indicative of an instantaneous outstanding transaction count based on outputs provided by said first and second mask circuits.

11. (Original) The increment/decrement circuit as recited in claim 10, wherein said instantaneous outstanding transaction count is forwarded to a counter circuit for further processing.

12-17. (Cancelled)

18. (Currently Amended) A computer system having an increment/ decrement circuit for use with a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the increment/decrement circuit comprising:

means for receiving and aligning ~~at least~~ a multi-bit block of said debug data;

means for ~~selectively asserting an increment signal based on~~ selecting a first portion of said block of aligned debug data;

means for ~~selectively asserting a decrement signal based on~~ selecting a second portion of said block of aligned debug data; and

means for generating an accumulated value using said first portion and said second portion. ~~based on said increment and decrement signals.~~

19. (Currently Amended) The computer system as recited in claim 18, wherein said means for generating an accumulated value is operable to forward a signal indicative of an instantaneous outstanding transaction count based on said first portion and said second portion. ~~increment and decrement signals.~~

20. (Original) The computer system as recited in claim 19, wherein said instantaneous outstanding transaction count is forwarded to a counter circuit for further processing relative to operations selected from the group consisting of latency calculations, advanced triggering, debug calculations, coverage calculations, and performance analysis.